

28th IEEE International Symposium on Asynchronous Circuits and Systems 16-19 July 2023, Beijing, China



Paper Deadlines

Regular papers 20 February 2023 (abstract registration) 27 February 2023 (paper submission)

18 April 2023 (notification of acceptance)

9 May 2023 (final version)

Industrial papers 30 April 2023 (paper submission)

Fresh Ideas 14 May 2023 (notification of acceptance)

28 May 2023 (final version)

Call for Papers

The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum for researchers and Industry to present their latest insights and results in asynchronous VLSI computing. Asynchronous computations are at the heart of recent deep learning and neuromorphic designs and well-suited for distributed tasks in high-performance low-energy processing and communication.

We invite you to submit 6-10 page regular papers or 4-page short papers with original scientific work relevant to ASYNC, in IEEE conference format (double-column, 10pt or larger). Author information must be omitted from the manuscripts. Accepted papers must be presented and will be published in the Symposium Proceedings and the IEEE Xplore Digital Library.

We also encourage you to submit 1-2 page papers for demo/poster/ideas with a demo/poster abstract or "fresh ideas" to try out live. These go through a light-weight review. Accepted papers must be presented and will be distributed as handouts at the Symposium.

We solicit 1-2 page papers from Industry on state-of-the-art integration of asynchronous designs to existing or emerging technologies. These must follow the format of a regular paper, but will go through a separate light-weight review process. Accepted papers must be presented and will be published in the Symposium Proceedings and the IEEE Xplore Digital Library.

General Co-Chairs

Hong CHEN

Tsinghua University, Beijing, China hongchen@tsinghua.edu.cn

Giacomo INDIVERI

ETH / University of Zürich, Switzerland giacomo@ini.uzh.ch

Program Co-Chairs

Laurent FESQUET

Grenoble Institute of Technology, France laurent.fesquet@univ-Grenoble-alpes.fr

Jia DI

University of Arkansas, USA idi@uark.edu

